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# Exercise 3:
# LVS

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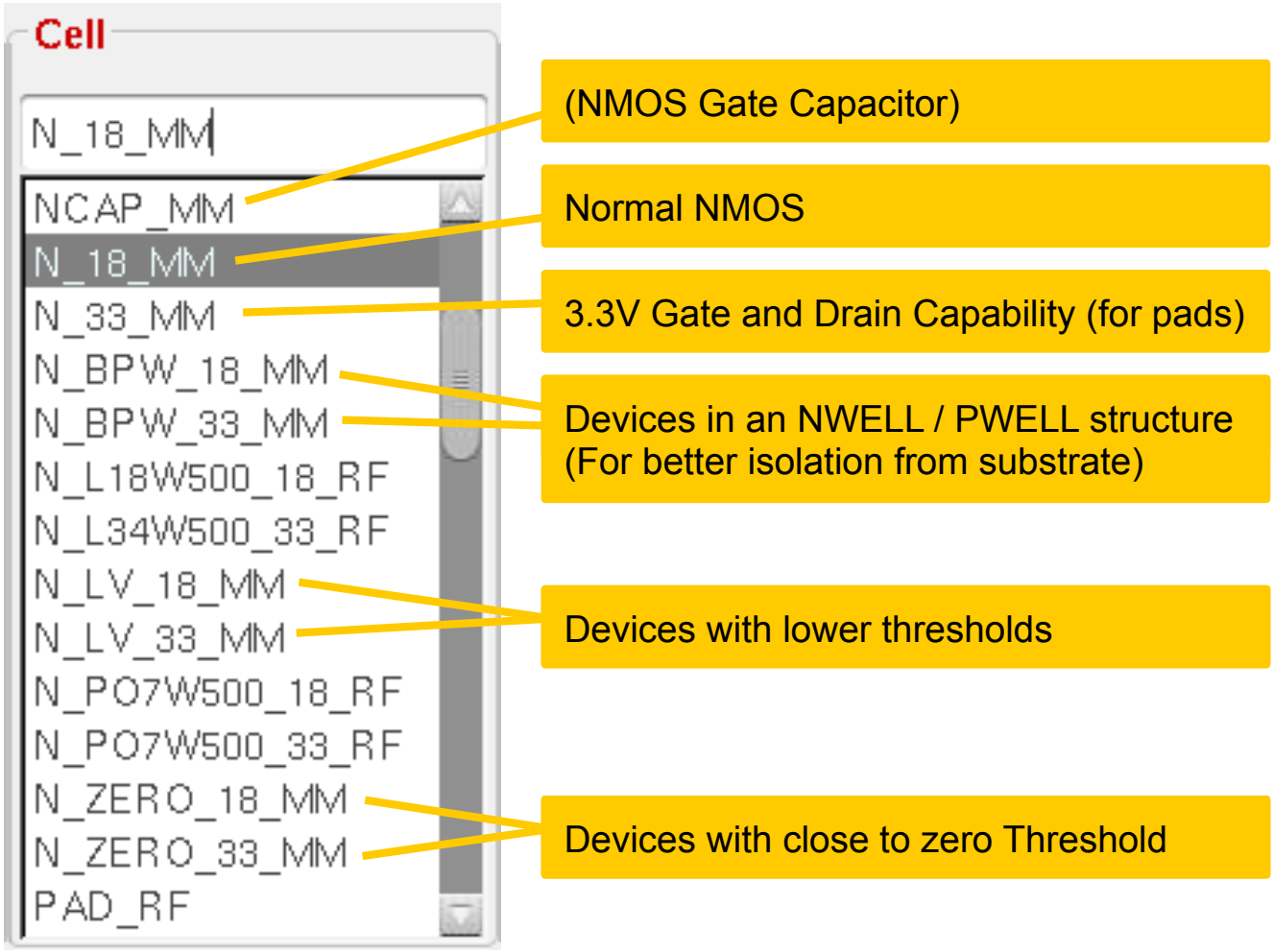
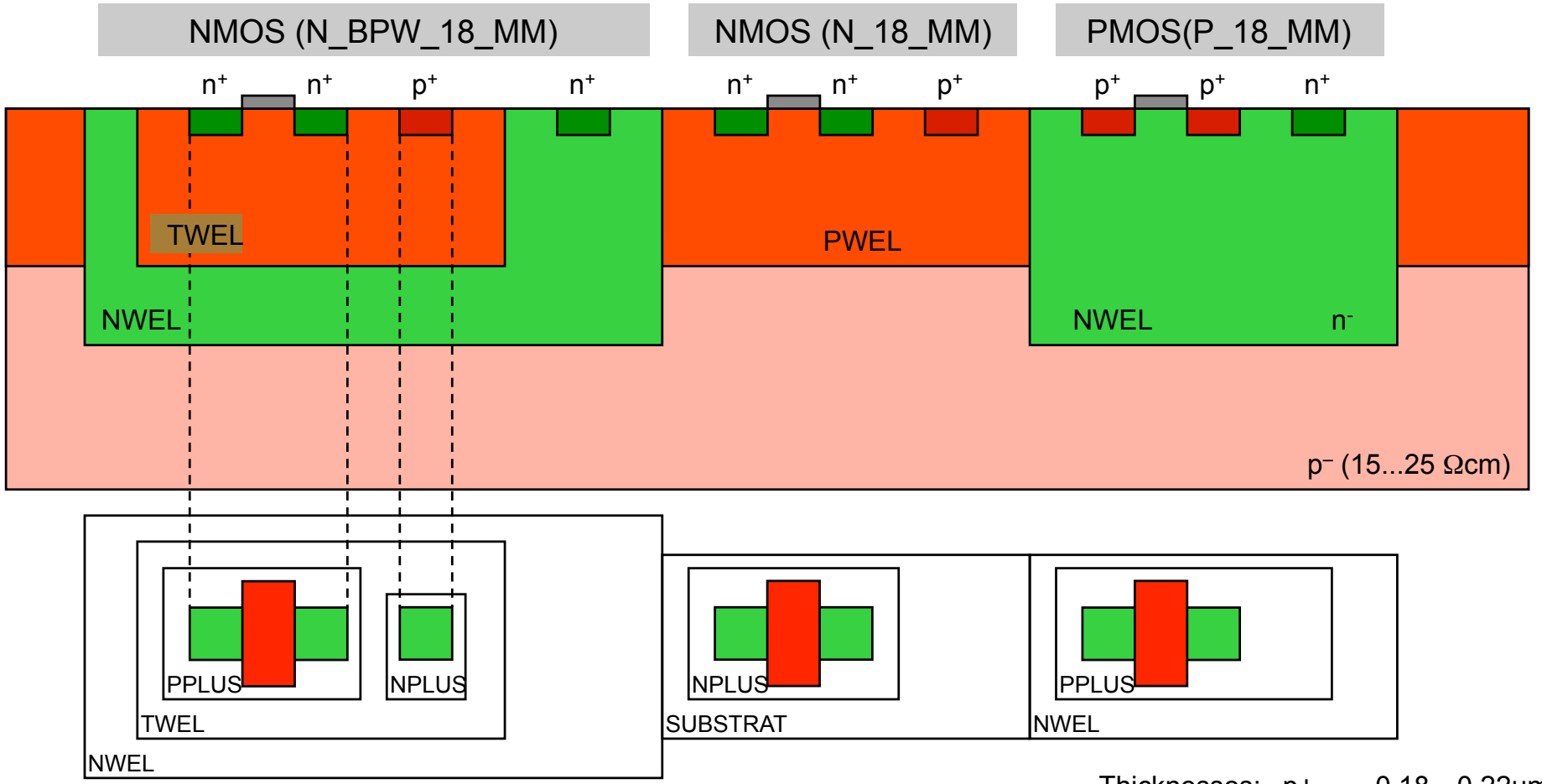
# DEVICES & LAYERS

# Devices

- The technology used offers several different NMOS and PMOS devices. For NMOS:



# Cross Sections of Devices




p-material

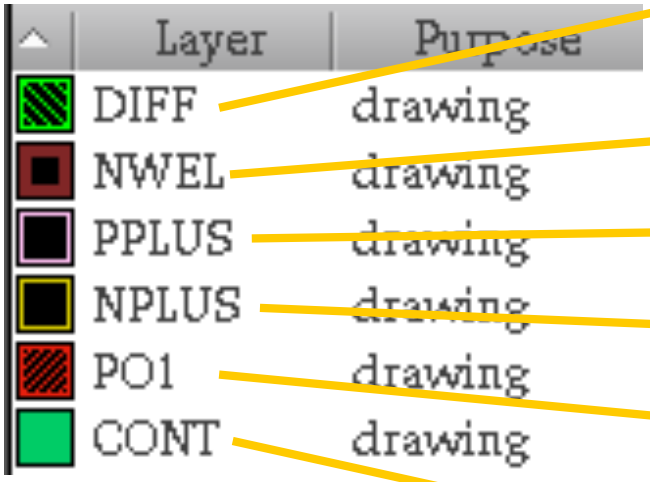
n-material

Thicknesses:

| | |
|---|---|
| p+ | 0.18…0.22µm |
| n+ | 0.16…0.20 µm |
| PWELL | ??? µm |
| TWELL | 1.0…1.4 µm |
| NWELL | 1.6…2.0 µm |

# Layers

- The most important *device* layers are




DIFFUSION:
implanted regions. The type (n++ or p++) if fixed by extra layers PPLUS or NPLUS

NWELL: Mostly for PMOS transistors

PPLUS: DIFFUSION surrounded by PPLUS is p++ region

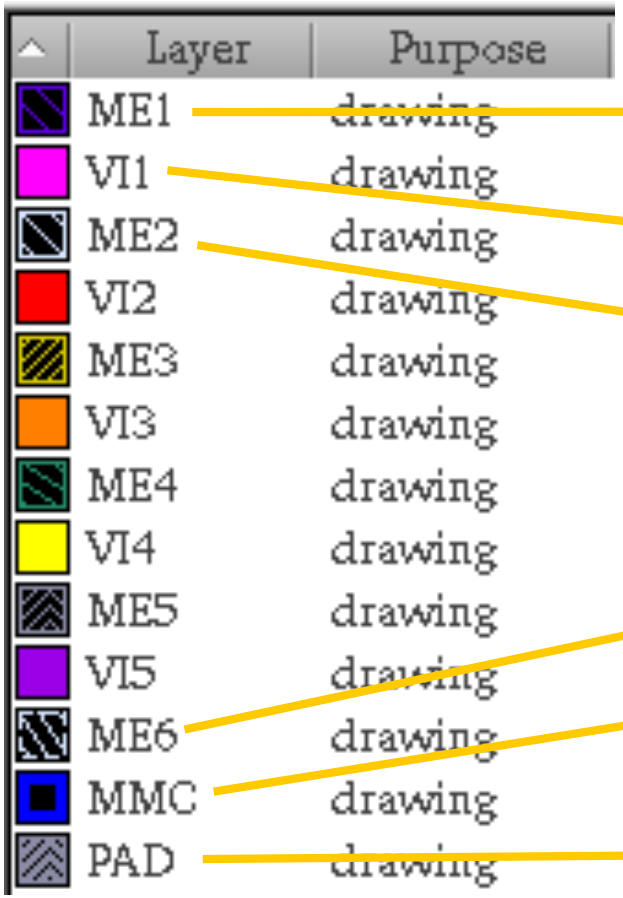
PPLUS: DIFFUSION surrounded by NPLUS is n++ region

POLY1: gates and first interconnect layer

CONT: connections between POLY1 or between DIFFUSION To first metal layer

# Layers

- The *routing* layers are




ME1: lowermost metal layer.
Connects to POLY1 or DIFFUSION via CONT

VI1 = VIA1: contacts metal1 to metal2

ME2: ...

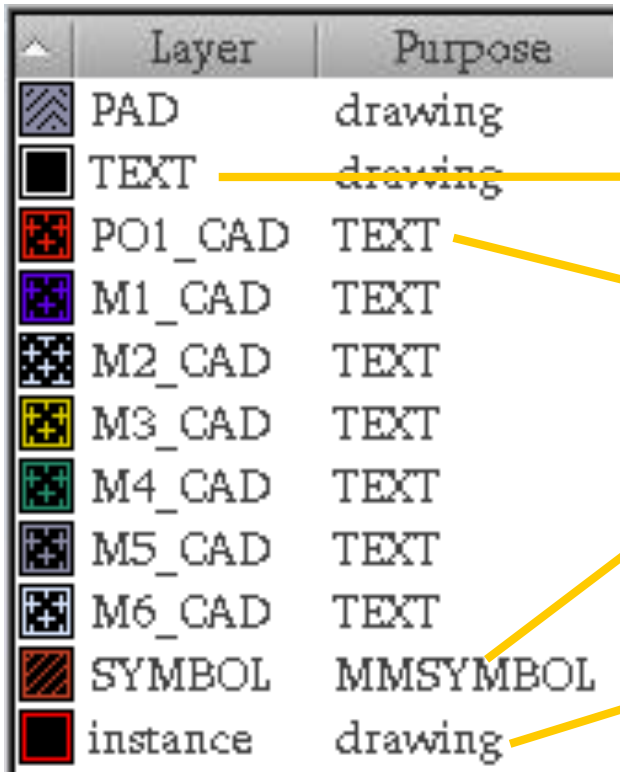
M6: Topmost metal

MMC: Extra metal layer between M5 and M6 (!) for MiM-Caps

PAD: Opening in chip passivation, leaving access to ME6

# Layers

- Some *other* layers are




TEXT: Can be used to comment layout
Not used for chip production

xx_CAD: used to label nets (see later)

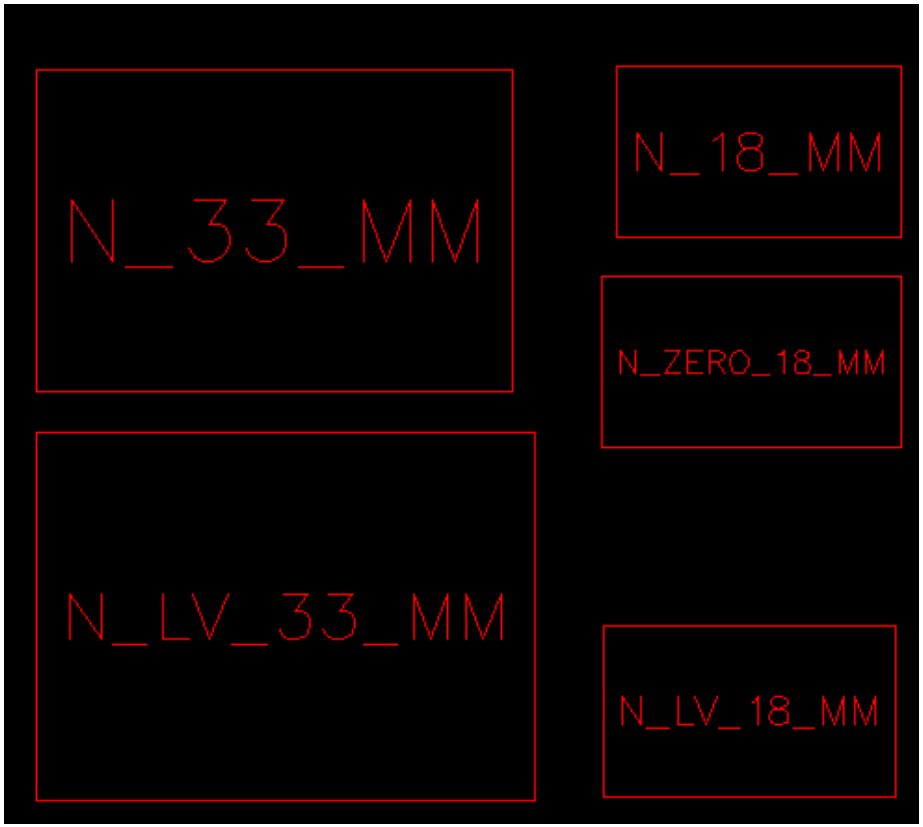
SYMBOL: Used to mark active devices (see later)

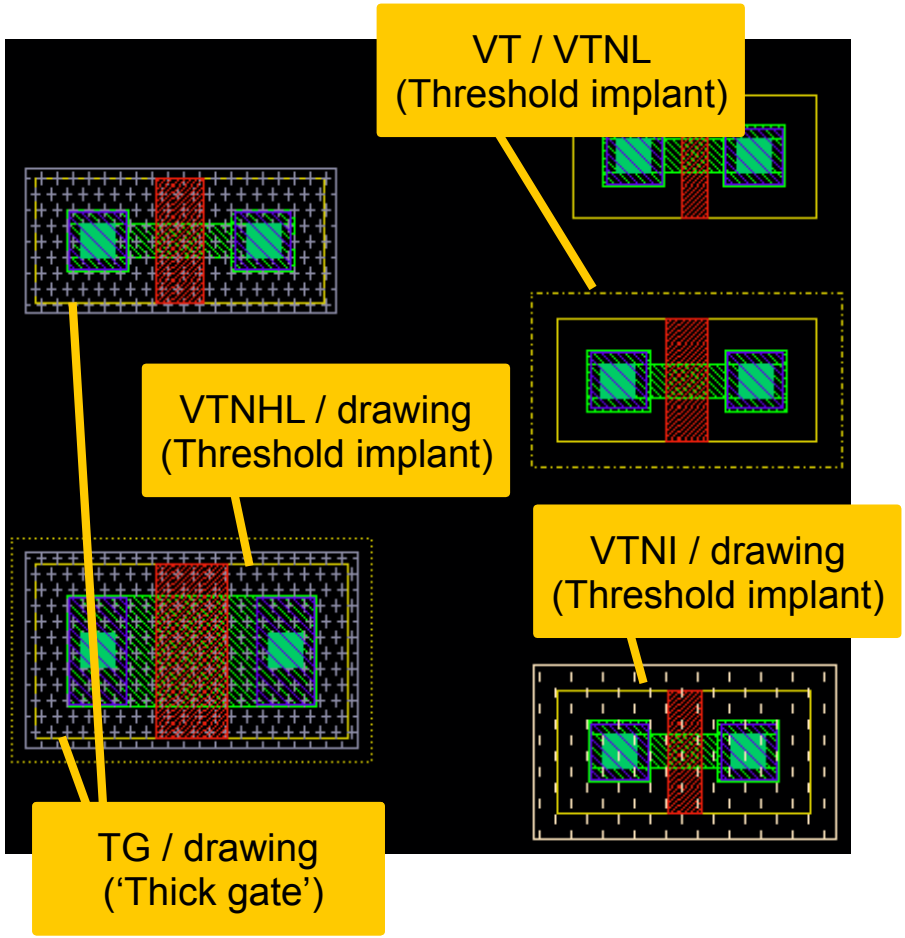
Instance: cadence layer. Used to display outline of a cell.
If drawn in a cell, defines outline to show
(otherwise, largest extent is used)

- There are many more layers, see *... Edit Valid Layers ...*

# Special Devices

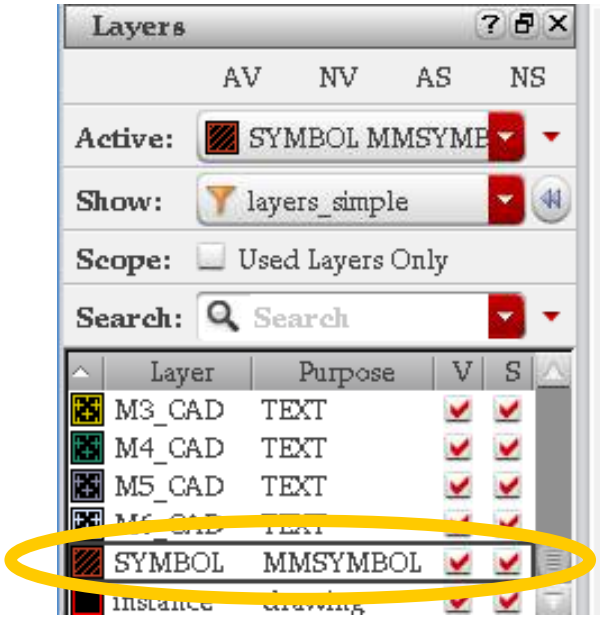
- The *various types* of NMOS / PMOS are identified by *extra layers* drawn on top of the device
- For the NMOS devices:

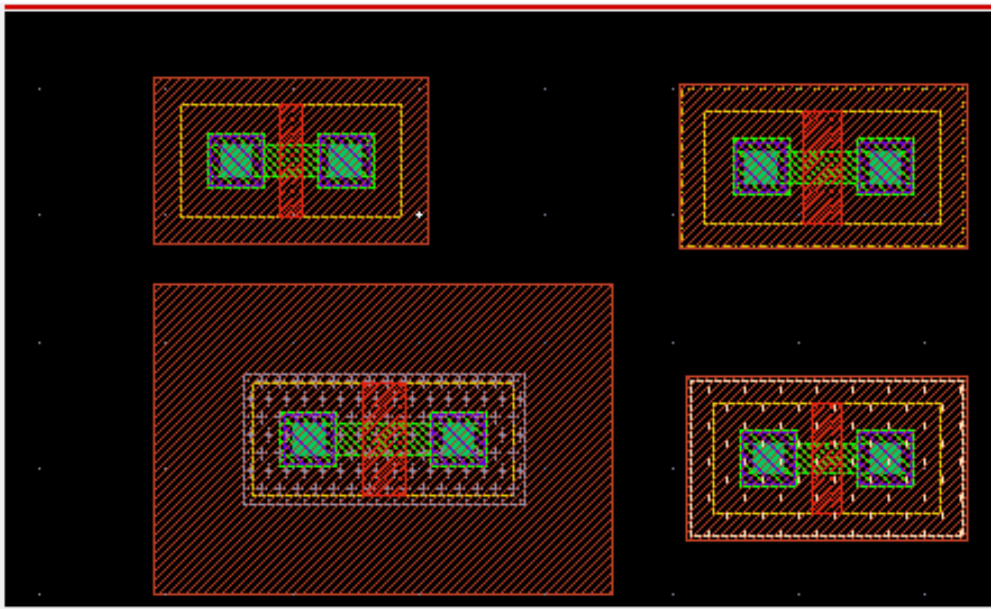


# The SYMBOL layer

- In this technology *ALL* active devices *MUST* be surrounded by the SYMBOL (MMSYMBOL) layer
  - This is SYMBOL / MOL in 'active Layer Display'
- If this layer is missing, extraction will *not* find the device!
- Most of the time, this layer is set invisible
  - and can therefore be easily forgotten!



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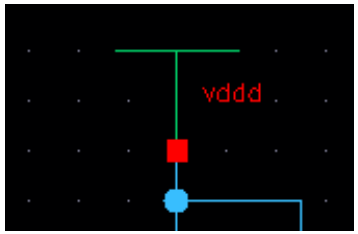
# LVS

# LVS: Layout Versus Schematic

- The LVS Tool checks that a layout corresponds to a given schematic
- It has 3 steps
  1. Extraction of a netlist from the schematic
  2. Extraction of a netlist from the layout
  3. Comparison of both netlists

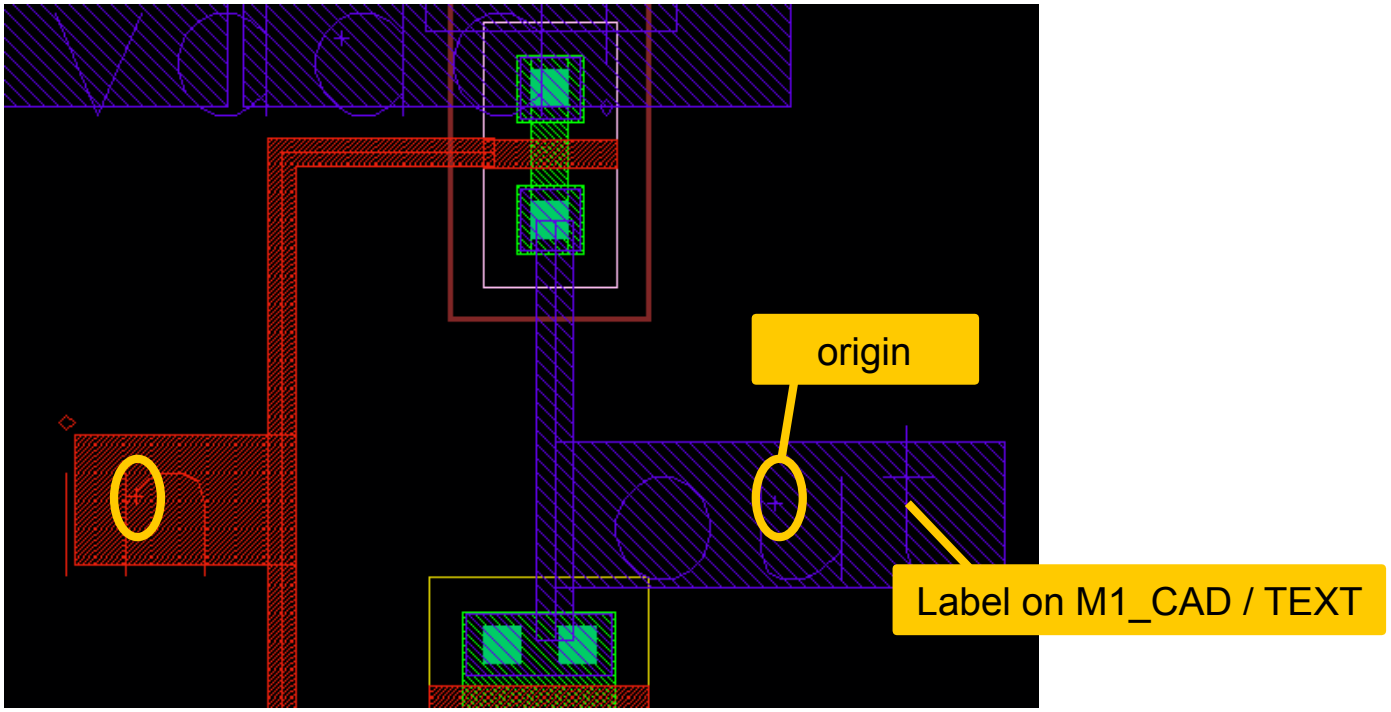
- The schematic is normally a ‘schematic’ view with the same cell name.
  - It can be a different view sometimes...

- Note that global nets are denoted by ‘!’.
  - For example, the vddd symbol from analogLib connects to net vddd!



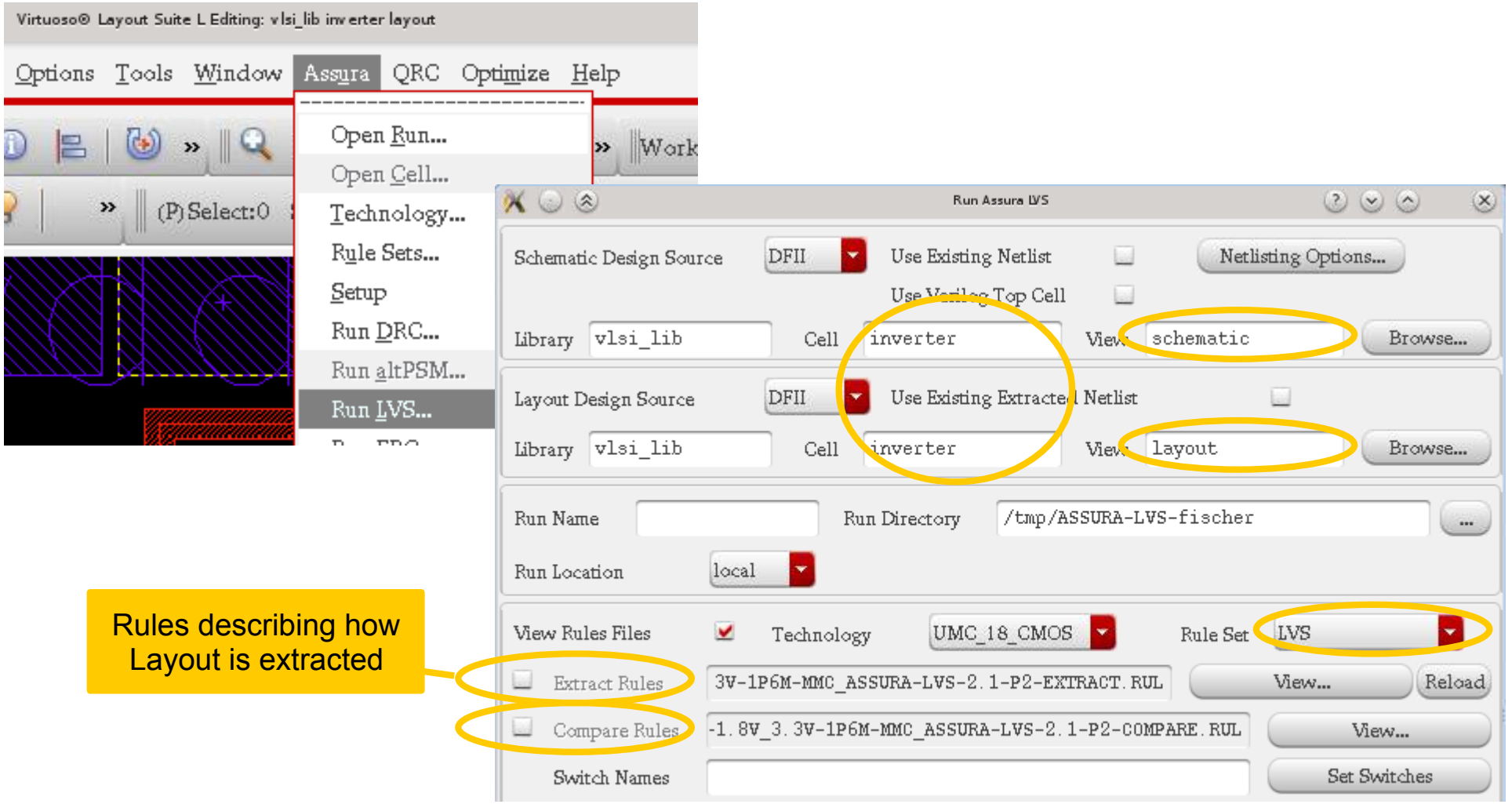
# Labels

- To *help* the LVS tool, the nets which are pins / supplies in the *schematic* should be *labelled* in the *layout*
- This is done by adding TEXT (Create → Label, 'l') on one of the PO1_CAD...M6_CAD/TEXT layers to a corresponding shape of the net
  - The ORIGIN of the label must touch the shape!



# Starting LVS

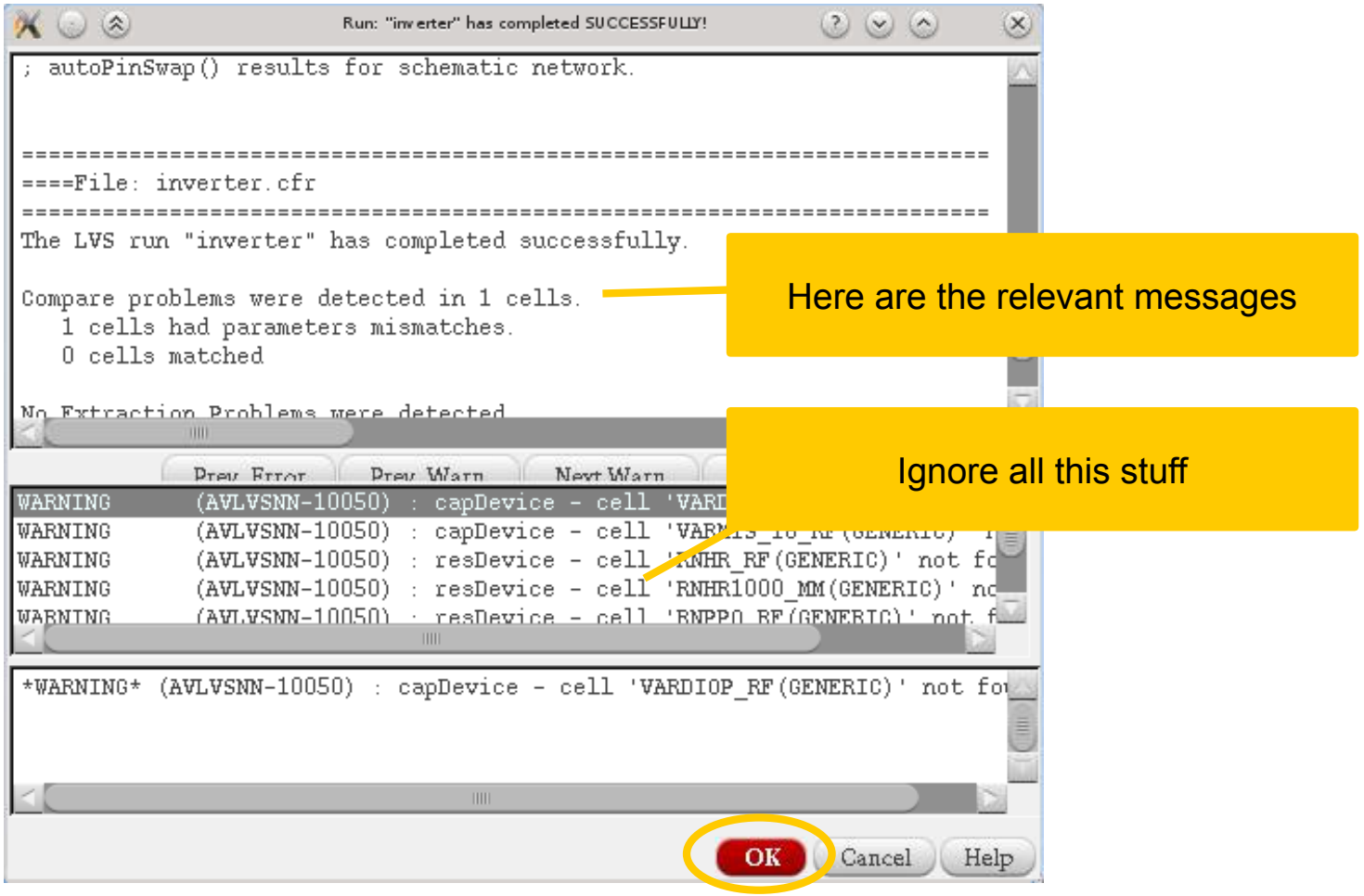
- Select from the top menu Assura → Run LVS
  - Make sure *Rule Set LVS* is selected




Rules describing how Layout is extracted

# LVS Overall Results

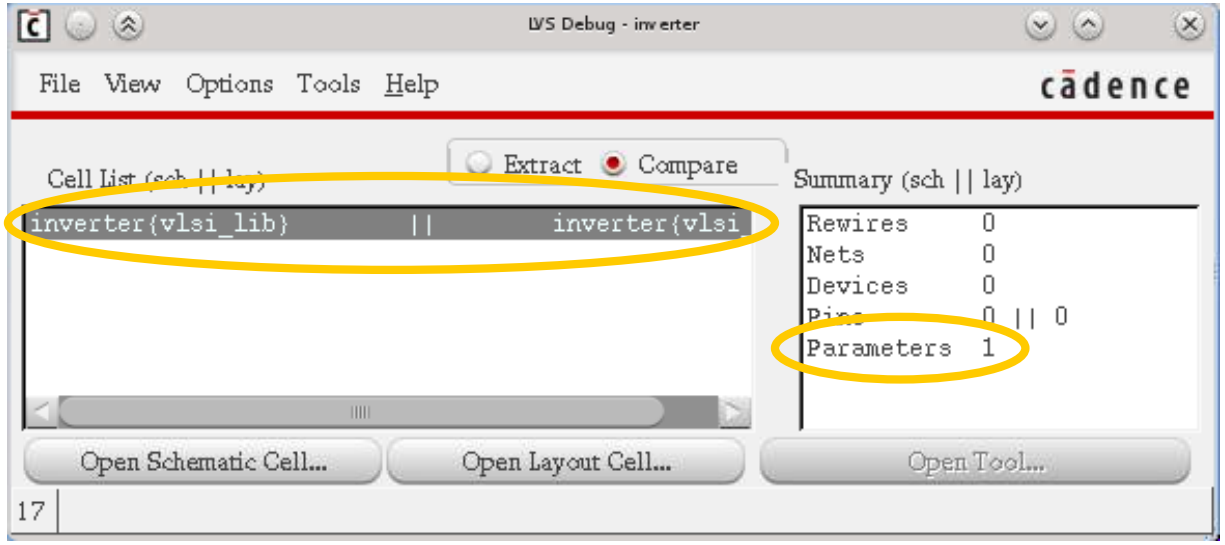
- If there are mismatches, you first get a warning window



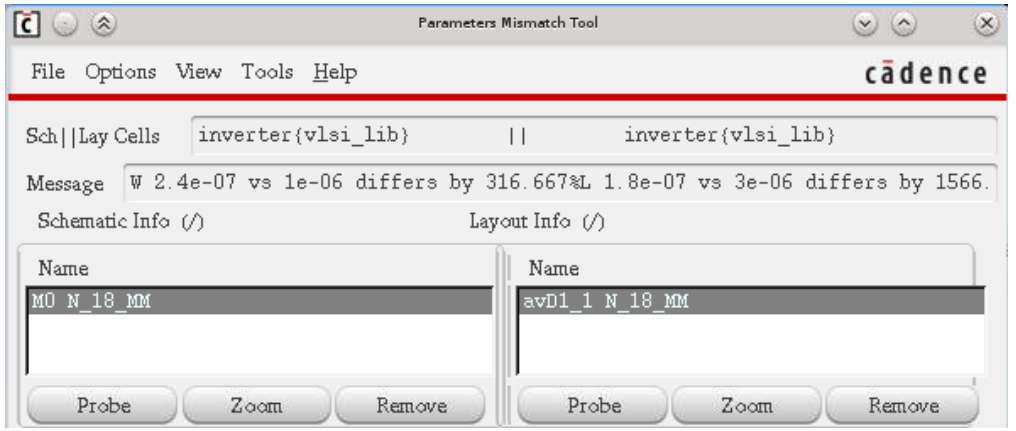

- Close it with ***OK***

# LVS Detail Results

- A new window opens
  - Select the cell to view error details

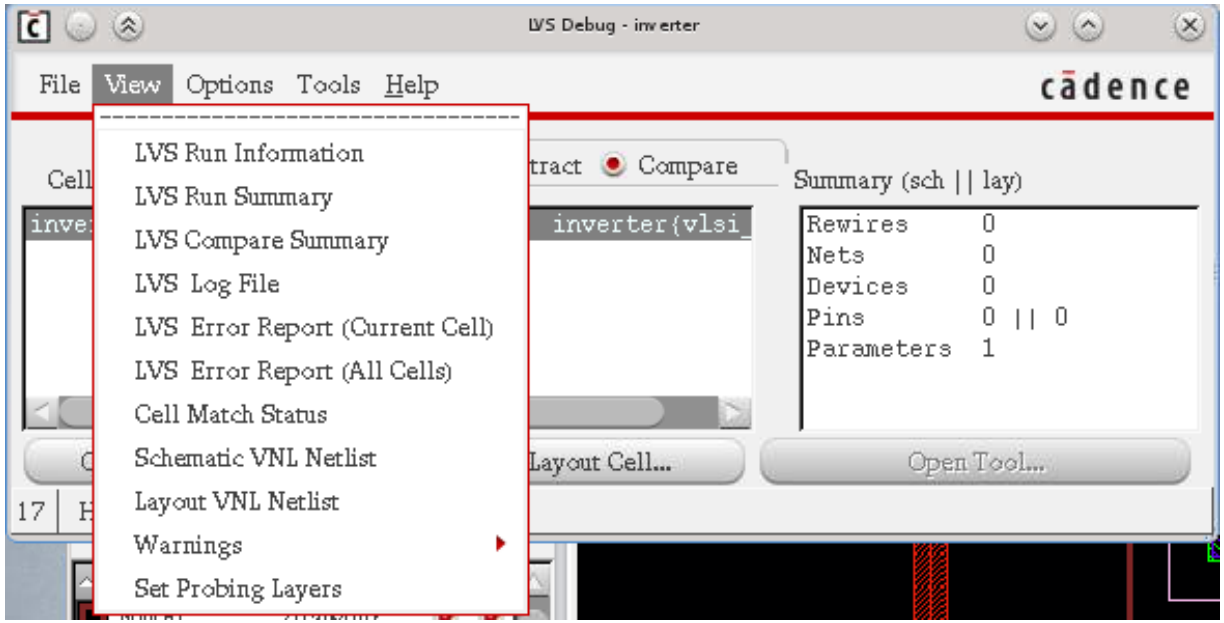



- Double click on the error type to see details
- Also use Options-> Show Details



# Viewing the Netlists

- You can see the generated netlists in the ‘View’ section



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# EXERCISES

# Exercise A: Inverter

- Generate the schematic of an inverter
  - Use the gnd symbol from analogLib for ground
  - Use the vddd symbol for the supply
  - Use an N_18_MM and a P_18_MM
  - Create pins for input and output

- Make a layout of the inverter
  - Do not try to make a nice layout (yet)
  - Use the MOS devices from lib UMC_18_CMOS
  - Make sure you add contacts (‘o’) to substrate and to the NWELL
  - Connect the substrate / well contacts to the correct supplies
  - Connect the gates / sources / drains correctly
  - Add label (‘l’) to input, output and the supplies

- Start an LVS

# Exercise B: NAND3

- Repeat the same for a NAND3 gate