RUPRECHT-KARLS-
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Exercise:
CAM - Part 1

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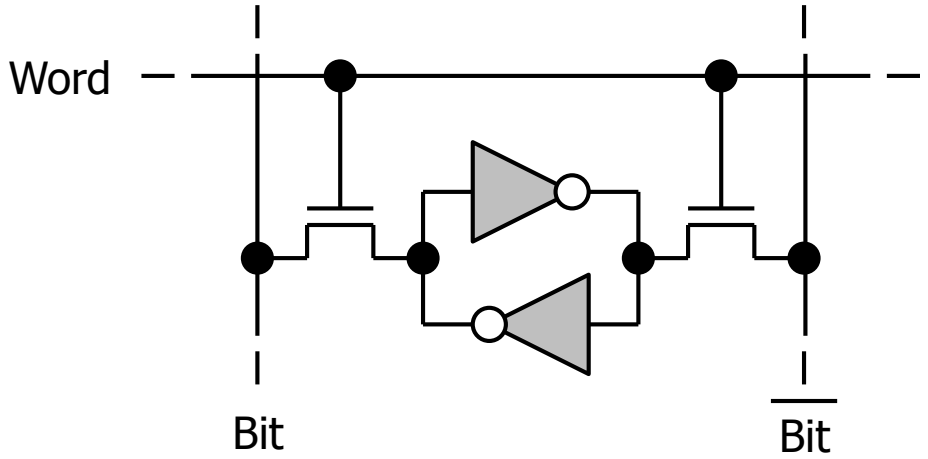
SRAM Cell

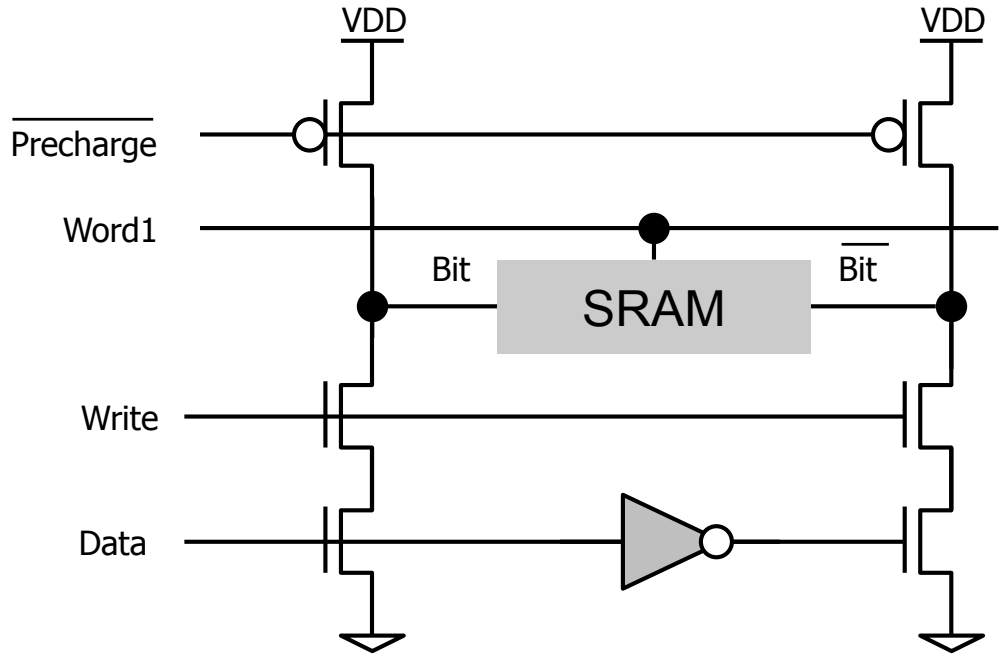
- Create the symbol of a SRAM cell



  - Pins should be: **`Bit, BitB, Word`**
- Make a schematic
  - Use global nets vdd! and gnd! for the supplies
  - Use minimal lengths for the NMOS
  - Use WNWRITE for the write NMOSs, WNINV for the others
  - Use WPINV and LPINV for the PMOSs
  - Start with W=0.44um for all MOS and min. length PMOS.

Simulating ONE SRAM cell

- Create the following schematic SIM_SRAM



  - Use wide (10 µm), minimum length MOS for driving
  - You can use a VCVS for the inverter
- Create control signals which
  - Write 0 to the SRAM, then read it back. Then try writing 1.
  - You can create a signal with multiple pulses by stacking vpulses
  - Use for instance 5ns for precharge

Simulating MULTIPLE cell

- Add a second SRAM cell
  - You also need a further control signal Word2
- Create signals for the following sequence
  - Write 0 to the first RAM cell
  - Write 1 to the second RAM cell
  - Read back the first cell
  - Read back the second cell
  - Make a drawing of the signals on paper first!
  - Work e.g. in steps of 5 ns
- Add additional capacitance to the bit lines until the circuit stops working

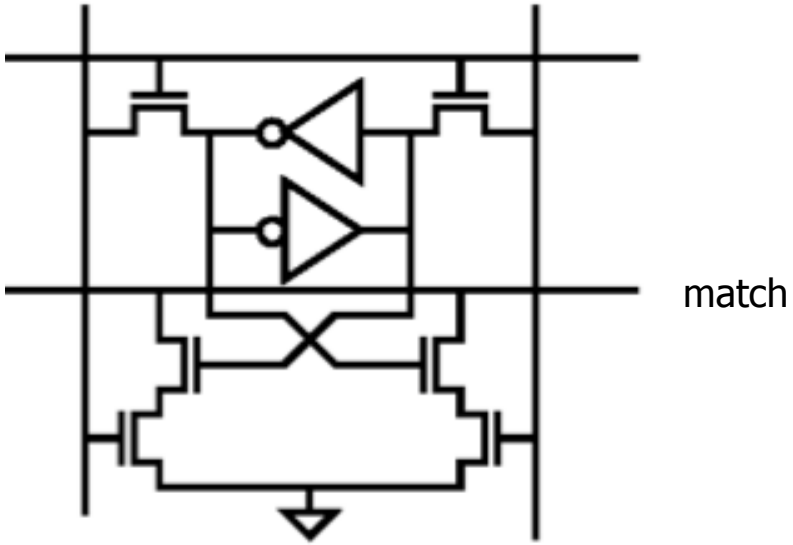
Transistor Dimensions

- Play with the dimensions of the transistors
- Find out in which ranges the cell works

- Add an OFFSET of 0.1V to one of the inverters in the SRAM cell (using a VDC source) and repeat the above exercise.

CAM Cell

- Starting from the SRAM cell, make a CAM cell



  - Add a **`Match`** signal
  - Use minimal length NMOS with WNMATCH
- Simulate the cell in schematic SIM_CAM:
  - Write 0 as before
  - Precharge the match line
  - Present comparison data at the bit lines (once matching, once mismatching)

Layout

- In the layout
  - Word and Match shall run horizontally
  - the two bit lines vertically
  - Power can go either way
  - No not put substrate or NWELL contacts in each CAM cell
  - Use only M1 - M3

- Before going in layout details, investigate on a paper various options for component and bus placement
  - Make sure cells can be placed directly adjacent to each other (maybe flipped or mirrored)
  - Try to minimize the NWELL area (and spacings) required
  - Keep your findings on 'good' (or 'bad') transistor sizes in mind!

- Do it!